STA8089FG

Fully Integrated GPS/Galileo/Glonass/BeiDou/QZSS Receiver with embedded RF and in-package Flash

Data brief

VFQFPN56 (7x7x0.85mm)

Features

- STMicroelectronics® positioning receiver with 48 tracking channels and 2 fast acquisition channels supporting GPS, Galileo, Glonass, BeiDou and QZSS systems
- Pin to pin compatible with STA8088FG
- Single die standalone receiver embedding RF Front-End and low noise amplifier
- -162 dBm indoor sensitivity (tracking mode)
- Fast TTFF < 1 s in Hot start and 30 s in Cold Start
- High performance ARM946 MCU (up to 196 MHz)
- 256 Kbyte embedded SRAM
- In-package SQI Flash Memory (16 Mbits)
- Real Time Clock (RTC) circuit
- 32-bit Watch-dog timer
- 3 UARTs
- 1 I^2C master/slave interface
- 1 Synchronous Serial Port (SSP, Motorola-SPI supported)
- USB2.0 full speed (12 MHz) with integrated physical layer transceiver
- 2 Controller Area Network (CAN)
- 2 channels ADC (10 bits)
- Operating condition:
  - Main voltage regulator (V_{INL}): 1.8 V ± 5%
  - Backup voltage (V_{INB}): 1.6 V to 4.3 V
  - Digital voltage (V_{DD}): 1.2 V ± 10%
  - RF core voltage (V_{CC}): 1.2 V ± 10%
  - IO Ring Voltage (V_{ddIO}): 1.8 V ± 5% or 3.3 V ± 10%
- Package:
  - VFQFPN56 (7 x 7 x 0.85 mm) 0.4 mm pitch
- Ambient temperature range: -40/+85°C

Description

STA8089FG is a single die standalone positioning receiver IC working on multiple constellations (GPS/Galileo/Glonass/BeiDou/QZSS).

The device is backward compatible with STA8088FG, this enables fast customer application migration.

The device is offered with a complete GNSS firmware which performs all GNSS operations including tracking, acquisition, navigation and data output with no need of external memories.

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1 Overview

STA8089FG is a highly integrated single-chip standalone GNSS receiver designed for positioning system applications.

STA8089FG embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including the US GPS, European Galileo, Russia's GLONASS, Chinese BeiDou and Japan's QZSS.

The STA8089FG ability of tracking simultaneously the signals from multiple satellites regardless of their constellation, make this chip capable of delivering exceptional accuracy in urban canyons and in the environments where buildings and other obstructions make satellite visibility challenging.

The STA8089FG is backward compatible with STA8088FG, enabling fast customer application migration.

The STA8089FG combines a high performance ARM946 microprocessor with I/O cpabilities and enhanced peripherals. It supports USB2.0 standard at full speed (12 Mbps) with on-chip PHY.

The device is offered with a complete firmware performing all positioning operations including acquisition, tracking, navigation and data output with no need of external memories.

The device powered with 1.8V enables the on-chip voltage regulators to internally supply the RF front-end, core logic and the backup logic. The device can be directly powered with 1.2 V bypassing the embedded voltage regulators which will be put in power down mode.

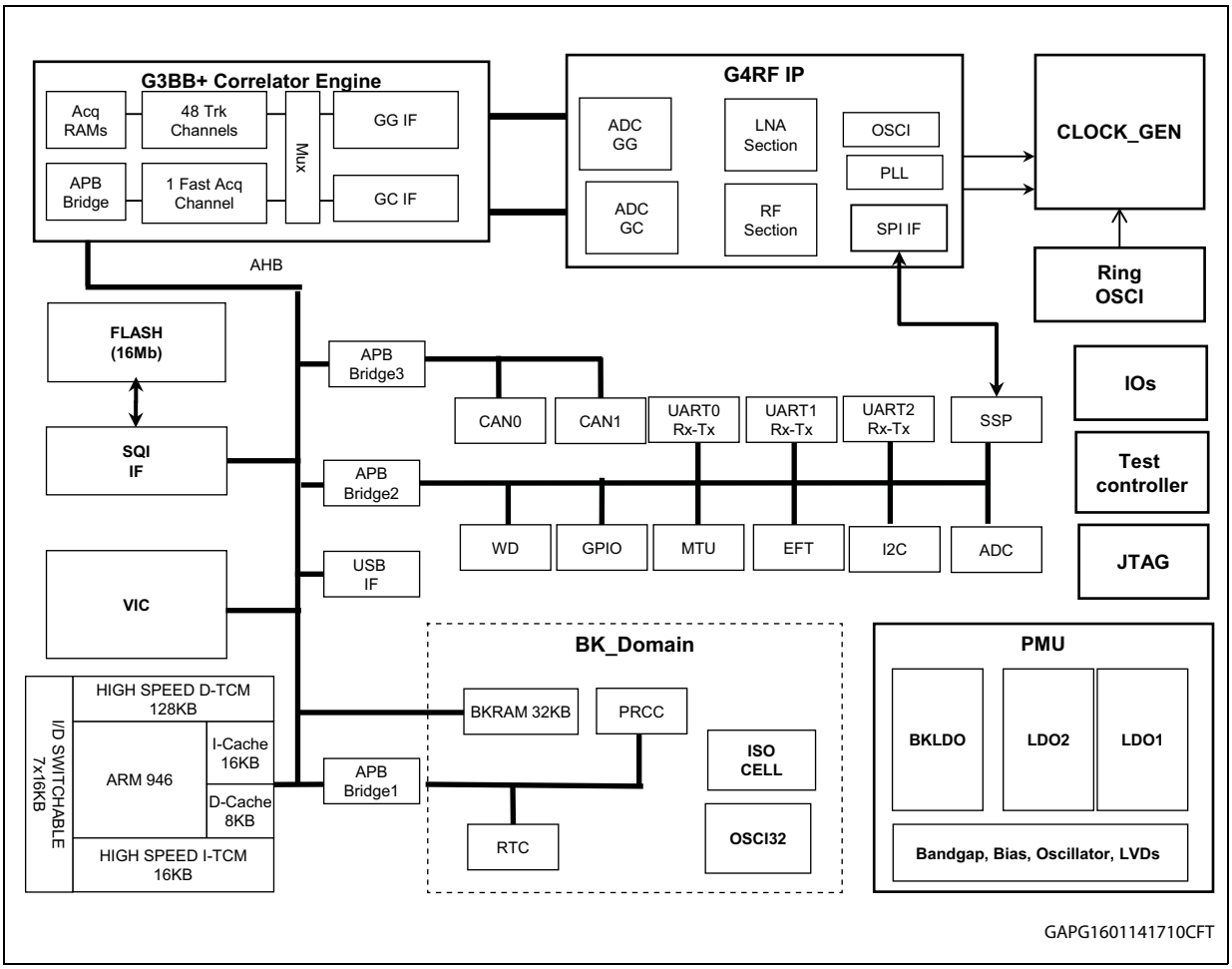
I/O lines are compatible with 1.8 V and 3.3 V.

The STA8089FG, using STMicroelectronics CMOSRF Technology, is housed in a VFQFPN-56 (7 x 7 x 0.85 mm) package with stacked 16 Mbit Flash memory.

2 Pin description

2.1 Block diagram

Figure 1. STA8089FG system block diagram



2.2 VFQFPN56 pin configuration

Figure 2. VFQFPN56 connection diagram (with CAN)

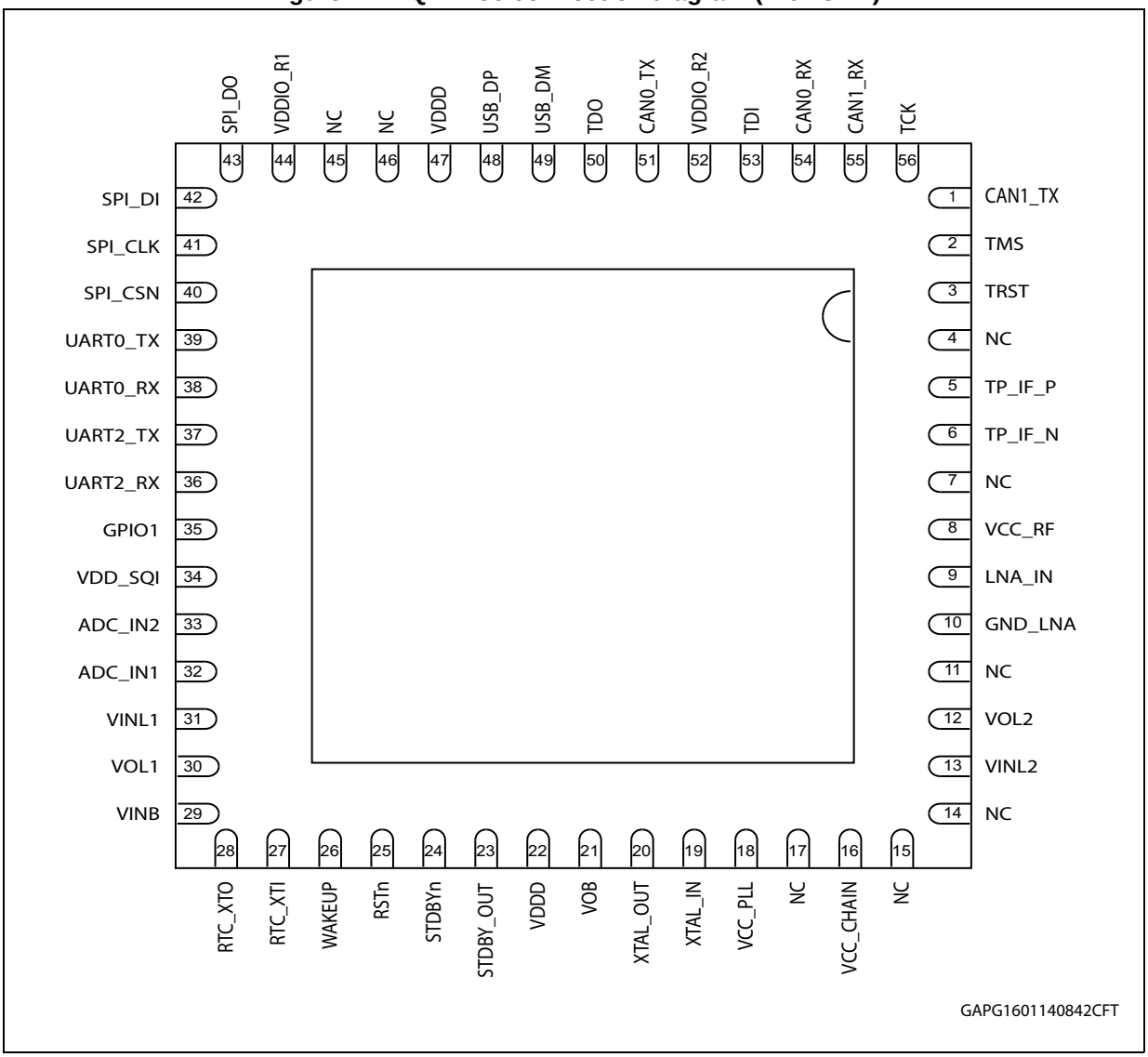
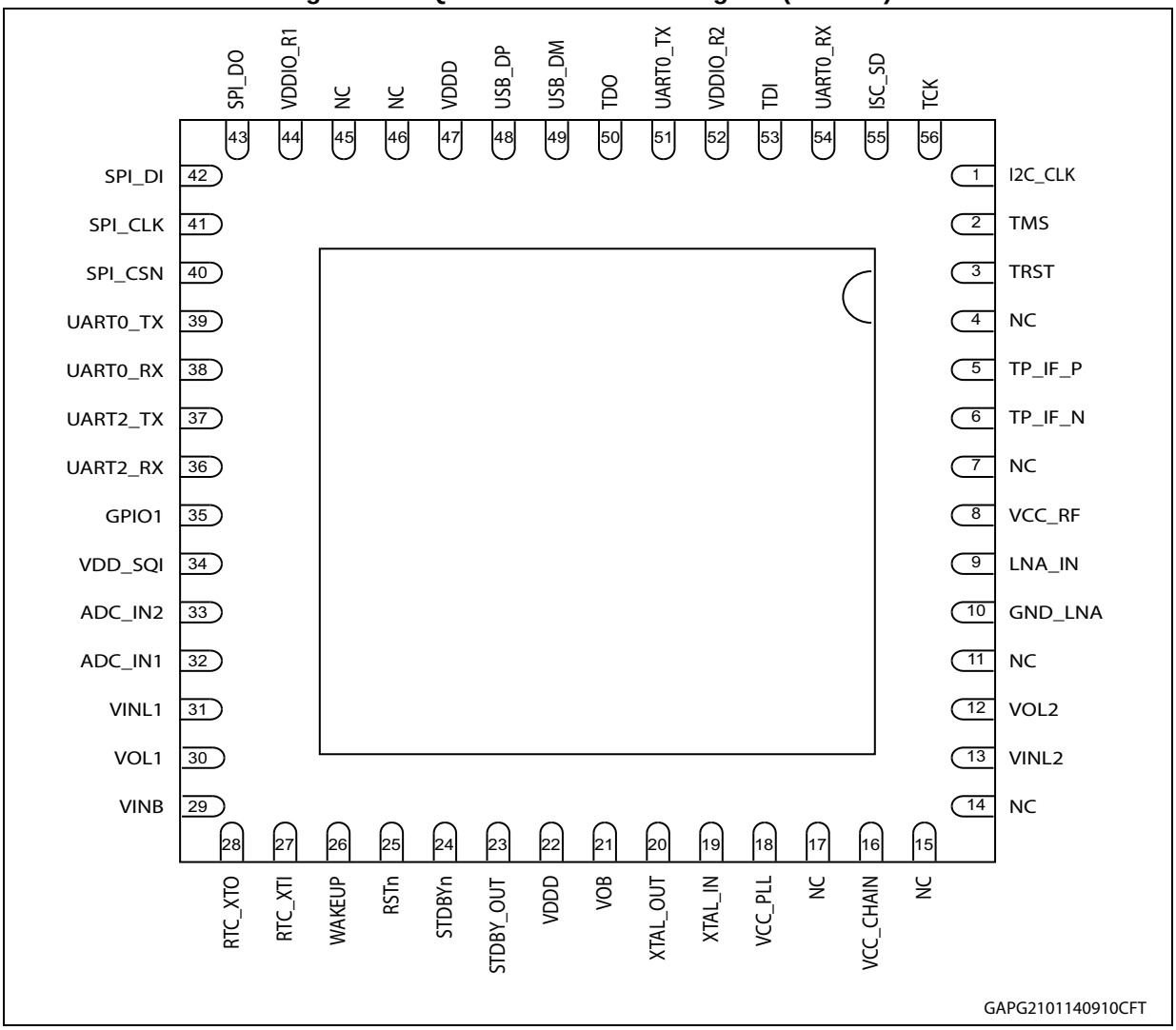


Figure 3. VFQFPN56 connection diagram (no CAN)



2.3 Power supply pins

Table 1. Power supply pins

Symbol	I/O voltage	I/O	Alternative function	Description	STA8089FG
VCC_CHAIN	1.2 V	PWR	default	Analog supply voltage for RF chain (1.2 V)	16
VCC_PLL	1.2 V	PWR	default	Analog supply voltage for PLL RF (1.2 V)	18
VCC_RF	1.2 V	PWR	default	Analog supply voltage for RF (1.2 V)	8
VDD_SQI	1.8 V	PWR	default	Digital supply voltage for SQI	34
VDDD	1.2 V	PWR	default	Digital supply voltage	22,47
VDDIO_R1	1.8 V or 3.3 V	PWR	default	Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V)	44

Table 1. Power supply pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Description	STA8089FG
VDDIO_R2	3.3 V	PWR	default	Digital supply voltage for I/O ring 2 (3.3 V)	52
VINB	1.6 V - 4.3 V	PWR	default	Backup LDO input supply voltage (1.6 V to 4.3 V)	29
VINL1	1.8 V	PWR	default	LDO1 input supply voltage (1.6 V to 4.3 V)	31
VINL2	1.8 V	PWR	default	LDO2 input supply voltage (1.6 V to 4.3 V)	13
VOB	1.0 V	PWR	default	LDO backup output voltage (1.0 V)	21
VOL1	1.2 V	PWR	default	LDO1 output voltage: 1.2 V or 1.8 V	30
VOL2	1.2 V	PWR	default	LDO2 output voltage (1.2 V)	12
GND	GND	GND	default	Ground	EP
GND_LNA	GND	GND	default	Ground	10

2.4 Main function pins

Table 2. Main function pins

Symbol	I/O voltage	I/O	Alternative function	Description	STA8089FG
ADC_IN1	1.4 V – 0 V typ range	I	default	ADC Analog input [1]	32
ADC_IN2	1.4 V – 0 V typ range	I	default	ADC Analog input [2]	33
RSTn	1.0 V	I	default	Reset Input with Schmitt-Trigger characteristics and noise filter.	25
RTC_XTI	1.4 V (max)	I	default	Input of the 32 KHz oscillator amplifier circuit and input of the internal real time clock circuit.	27
RTC_XTO	1.4 V (max)	O	default	Output of the oscillator amplifier circuit.	28
STDBY_OUT	1.0 V	O	default	When low, indicates the chip is in Standby mode	23
STDBYn	1.0 V	I	default	When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply	24
WAKEUP	1.0 V	I	default	WAKEUP from STANDBY mode	26

2.5 Test/emulated dedicated pins

Table 3. Test/emulated dedicated pins

Symbol	I/O voltage	I/O	Alternative function	Description	STA8089FG
TCK	VDDIO_R2	I	default	JTAG Test Clock	56
TDI	VDDIO_R2	I	default	JTAG Test Data In / BOOT3	53
TDO	VDDIO_R2	O	default	JTAG Test Data Out	50
TMS	VDDIO_R2	I	default	JTAG Test Mode Select / BOOT2	2
TP_IF_N	1.2 V	O	default	Diff.Test Point for IF – Neg.	6
TP_IF_P	1.2 V	O	default	Diff.Test Point for IF . Pos.	5
TRSTN	VDDIO_R2	I	default	JTAG Test Circuit Reset	3

2.6 Communication interface pins

Table 4. Communication interface pins

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8089FG
CAN0_RX(1)	VDDIO_R2	I	AF0 (default)	CAN0_RX	CAN0 receive data input	54
		I	AF1	UART0_RX	UART0 Rx data	
		I	AF2	Tsense	External temperature capture port	
		I/O	AF3	I2C_SD	I2C serial data	
CAN0_TX(1)	VDDIO_R2	O	AF0 (default)	CAN0_TX	CAN0 transmit data output	51
		O	AF1	UART0_TX	UART0 Tx data	
		I/O	AF2	GPIO7	General purpose I/O #7	
		O	AF3	I2C_CLK	I2C clock	
CAN1_RX(1)	VDDIO_R2	I/O	AF0	I2C SD	I2C serial data	55
		I/O	AF1	GPIO9	General purpose I/O #9	
		I	AF2 (default)	CAN1_RX	CAN1 receive data input	
		I	AF3	SQI_CEN	SQI Flash chip enable	
CAN1_TX(1)	VDDIO_R2	O	AF0	I2C_CLK	I2C clock	1
		I/O	AF1	GPIO8	General purpose I/O #8	
		O	AF2 (default)	CAN1_TX	CAN1 transmit data output	
		O	AF3	SPI_CSN	SPI chip select active low	

Table 4. Communication interface pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8089FG
SPI_CLK	VDDIO_R1	O	AF0 (default)	SPI_CLK	SPI clock	41
		I/O	AF1	GPIO25	General purpose I/O #25	
		O	AF2	SQI_CLK	SQI Flash clock	
		O	AF3	MMC_CLK	Multimedia Clock line	
SPI_CSN	VDDIO_R1	O	AF0 (default)	SPI_CSN	SPI chip select active low// IO_Power Sel Ring 1	40
		I/O	AF1	GPIO24	General purpose I/O #24	
		I	AF2	SQI CEN	SQI Flash chip enable	
		I/O	AF3	MMC_CMD	Multimedia card command line	
SPI_DI	VDDIO_R1	I	AF0 (default)	SPI_DI	SPI serial data input	42
		I/O	AF1	GPIO26	General purpose I/O #26	
		I/O	AF2	SQI_SIO0/SI	SQI Flash data IO 0 / ser. I	
		I/O	AF3	MMC_D0	Multimedia card data 0	
SPI_DO	VDDIO_R1	O	AF0 (default)	SPI_DO	SPI serial data output	43
		I/O	AF1	GPIO27	General purpose I/O #27	
		I/O	AF2	SQI_SIO1/SO	SQI Flash data IO 1 / ser. O	
		I/O	AF3	MMC_D1	Multimedia card data 1	
UART0_RX	VDDIO_R1	I	AF0 (default)	UART0_RX	UART0 Rx data	38
		I/O	AF1	GPIO30	General purpose I/O #30	
		I/O	AF2	SQI_SIO2	SQI Flash data IO 2	
		I	AF3	Timer_ICAPA	Extended function timer - input capture A	
UART0_TX	VDDIO_R1	O	AF0 (default)	UART0_TX	UART0 Tx data / BOOT1	39
		I/O	AF1	GPIO31	General purpose I/O #31	
		I/O	AF2	SQI_SIO3	SQI Flash data IO 3	
		O	AF3	Timer_OCMPA	Extended Function Timer – Output Compare A	
UART2_RX	VDDIO_R1	I	AF0 (default)	UART2_RX	UART2 Rx data	36
		I/O	AF1	GPIO28	General purpose I/O #28	
		I/O	AF2	I2C_SD	I2C serial data	
		I/O	AF3	MMC_D2	Multimedia card data 2	

Table 4. Communication interface pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8089FG
UART2_TX	VDDIO_R1	O	AF0 (default)	UART2_TX	UART2 Tx data / BOOT0	37
		I/O	AF1	GPIO29	General purpose I/O #29	
		O	AF2	I2C_CLK	I2C clock	
		I/O	AF3	MMC_D3	Multimedia card data 2	
USB_DM	VDDIO_R2	USB	AF0 (default)	USB_DM	USB D- signal	49
USB_DP	VDDIO_R2	USB	AF0 (default)	USB_DP	USB D+ signal	48

1. Only for STA8089FGB.

2.7 General purpose pins

Table 5. General purpose pins

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8089FG
GPIO1	VDDIO_R1	I/O	AF0 (default)	GPIO1	General purpose I/O #1	35
		I	AF1	MSPin_sdata	MSP serial data input	
		O	AF2	PPS_OUT	Pulse per second output	
		I	AF3	Tsense	External temperature capture port	

2.8 RF front-end pins

Table 6. RF front-end pins

Symbol	I/O voltage	I/O	Alternative function	Description	STA8089FG
LNA_IN	1.2 V	I	default	Low Noise Amplifier Input	9
XTAL_IN	1.2 V	I	default	Input Side of Crystal Oscillator or TCXO Input	19
XTAL_OUT	1.2 V	O	default	Output Side of Crystal Oscillator	20

3 Package and packing information

3.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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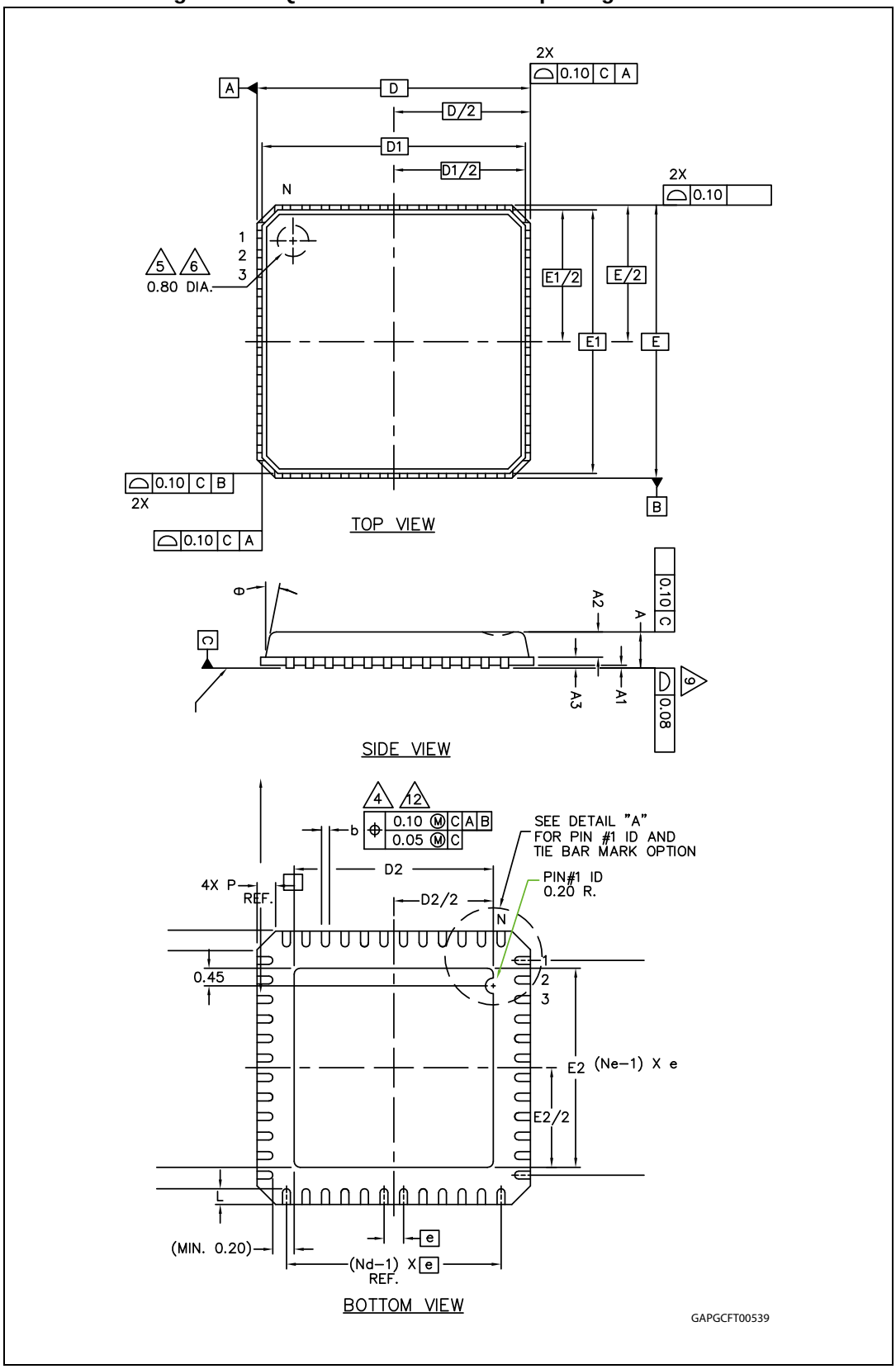
3.2 VFQFPN56 7 x 7 x 0.85 mm package information

Table 7. VFQFPN56 package dimensions

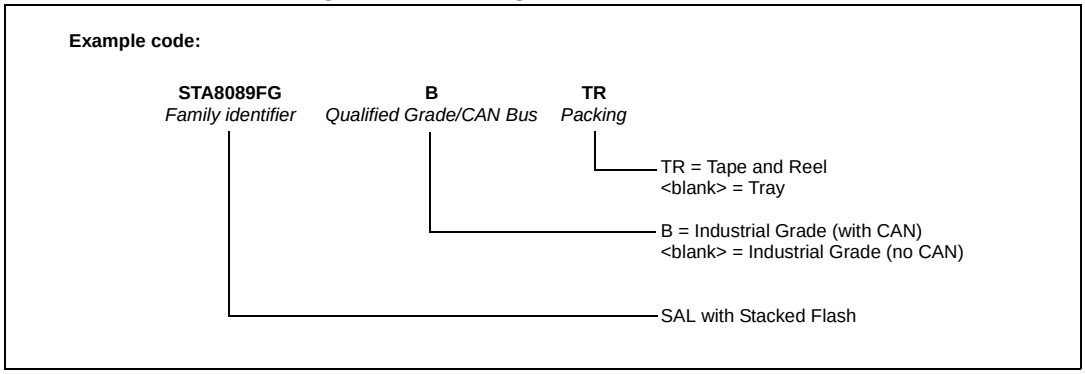
Symbol	Min.	Typ.	Max
Common dimensions			
A	0.80	0.85	0.90
A1	0	0.01	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
D		7.00 BSC	
D1		6.75 BSC	
D2	5.0	5.1	5.2
E		7.00 BSC	
E1		6.75 BSC	
E2	5.0	5.1	5.2
e		0.40 BSC	
θ	0°		12°
L	0.30	0.40	0.50
N		56	
Nd		14	
Ne		14	
P	0.24	0.42	0.60
Q	0.30	0.40	0.65
R	0.13	0.17	0.23

Figure 4. VFQFPN56 7 x 7 x 0.85 mm package dimension



4 Ordering information

Figure 5. Ordering information scheme



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
19-Dec-2013	1	Initial release.
31-Jan-2014	2	Updated *Features* list Updated following chapters: – *Chapter 1: Overview* – *Chapter 2: Pin description* – *Chapter 3: Package and packing information* – *Chapter 4: Ordering information*

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